

Energy efficient computing at Intel

George Bourianoff

Intel Corp

June 11, 2009

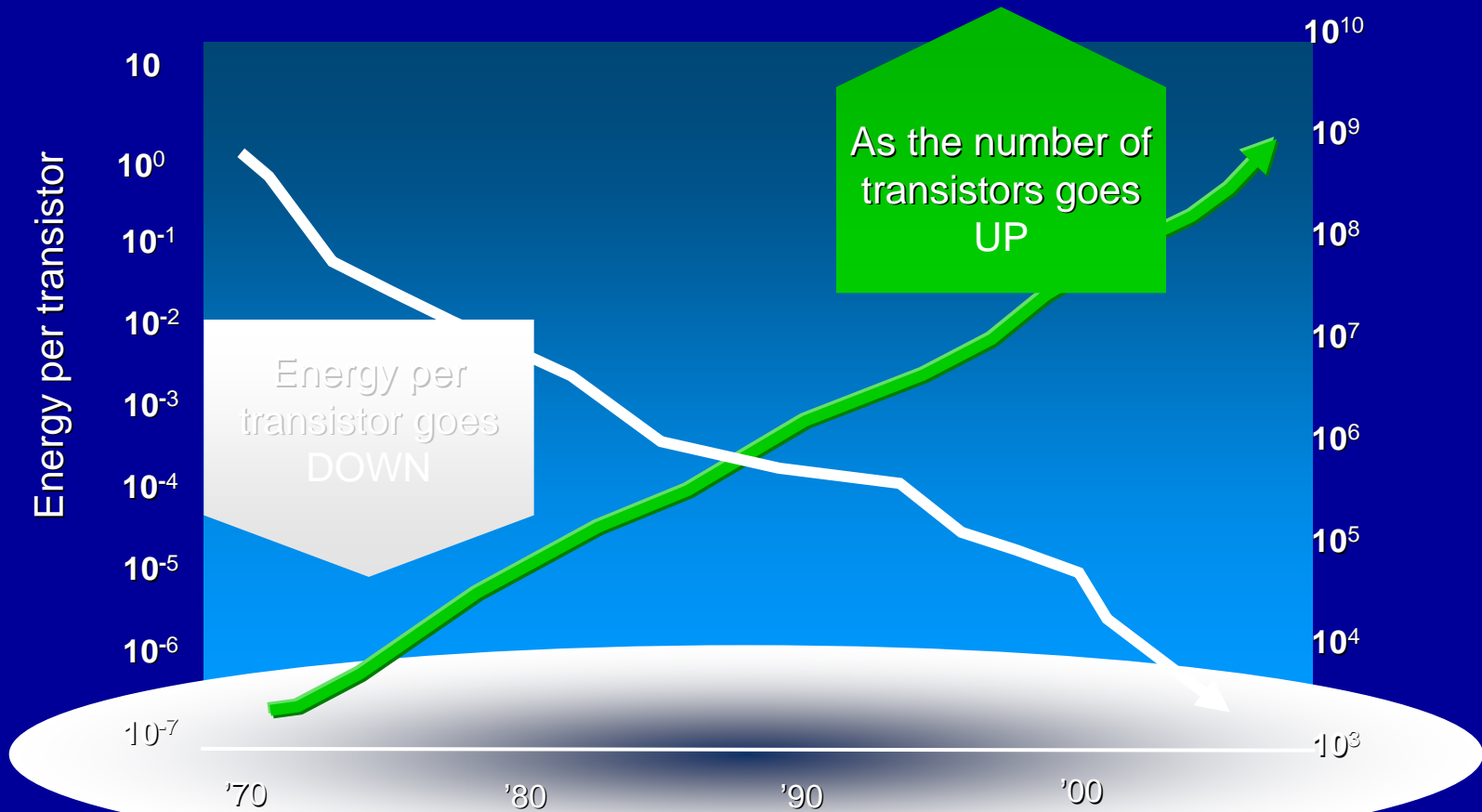
Key messages

- To extend Moore's law, Intel is addressing energy at all platform levels
- Intel is making steady progress in low power systems, platforms, interconnects and devices
- Intel is collaborating with the external research community to develop novel, beyond CMOS low power device research

Outline

- Introduction
 - Moore's law
 - Current status
- Steady progress in low power CMOS devices
 - 45 nm HK-MG for low power
 - High mobility, low power III-V devices
 - CNTs and graphene devices
 - Tunneling devices
- Exploration of low power beyond CMOS technology
 - Spin devices
 - Phase change devices and materials
 - Pseudo spintronics devices
- Conclusion

Moore's Law applied to energy



~ 1 Million Factor Reduction In Energy/Transistor Over 30+ Years

Source: WSTS/Dataquest/Intel

Moore's Law: Delivering Data Center Optimization



2002

- 3.7 TFlops
- 25 racks
- 512 Servers
- 1000 sq ft
- 128 kW

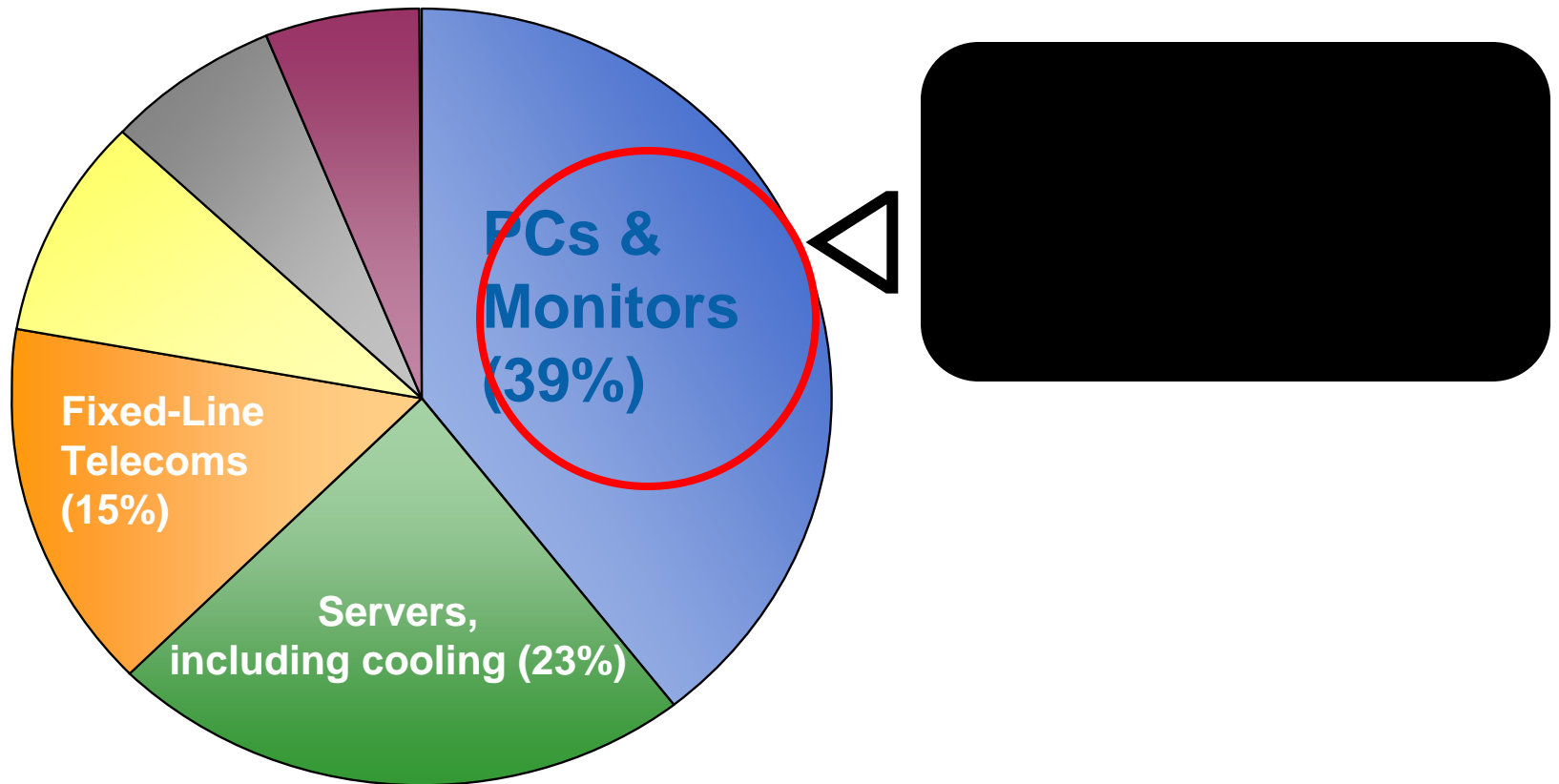


2007

- 3.7 TFlops
- 1 rack
- 53 Blades
- 40 sq ft
- 21 kW

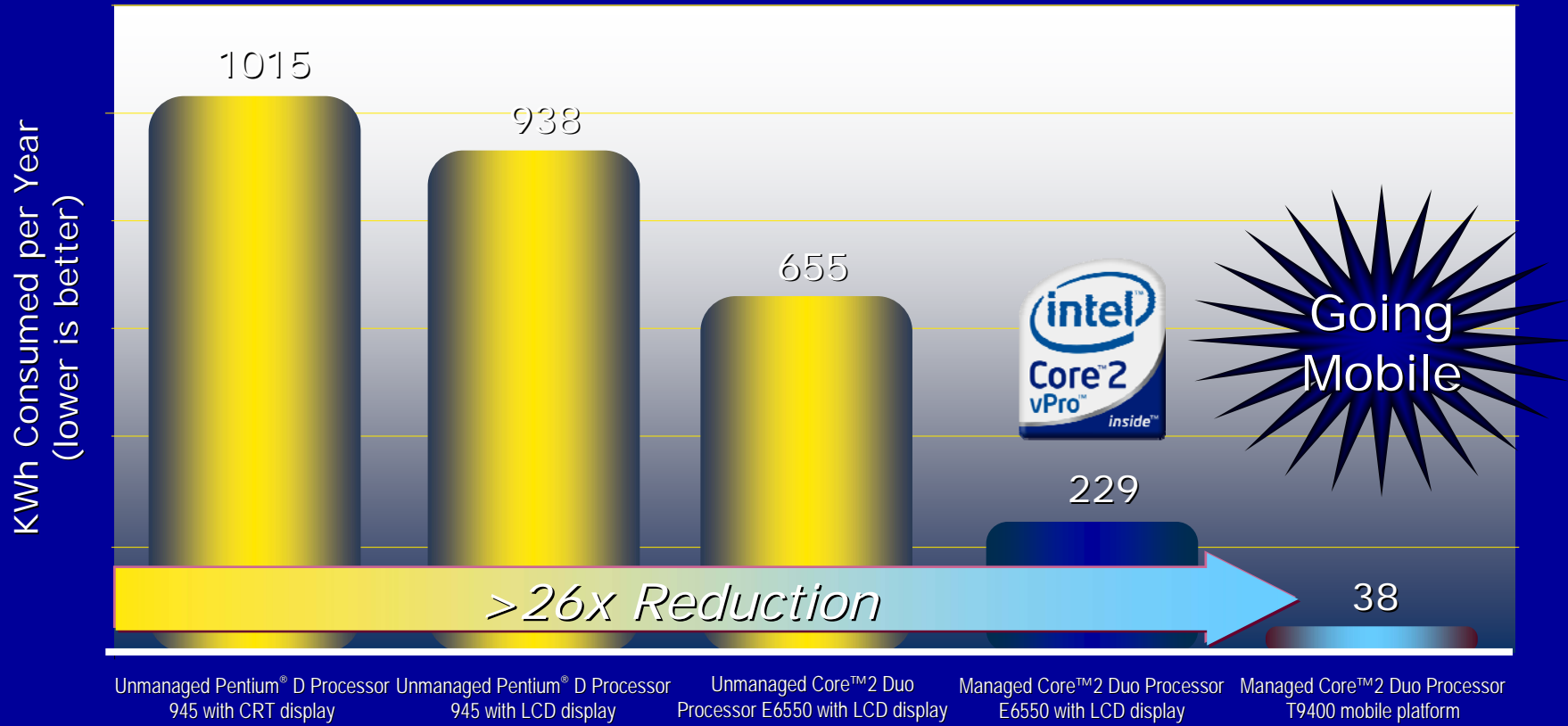


PC Energy Consumption is dominant



Potential Energy Savings Enabled by Moore's Law

Estimated Annual Energy Consumption



Energy savings comes from combination of transistor scaling and architectural innovations

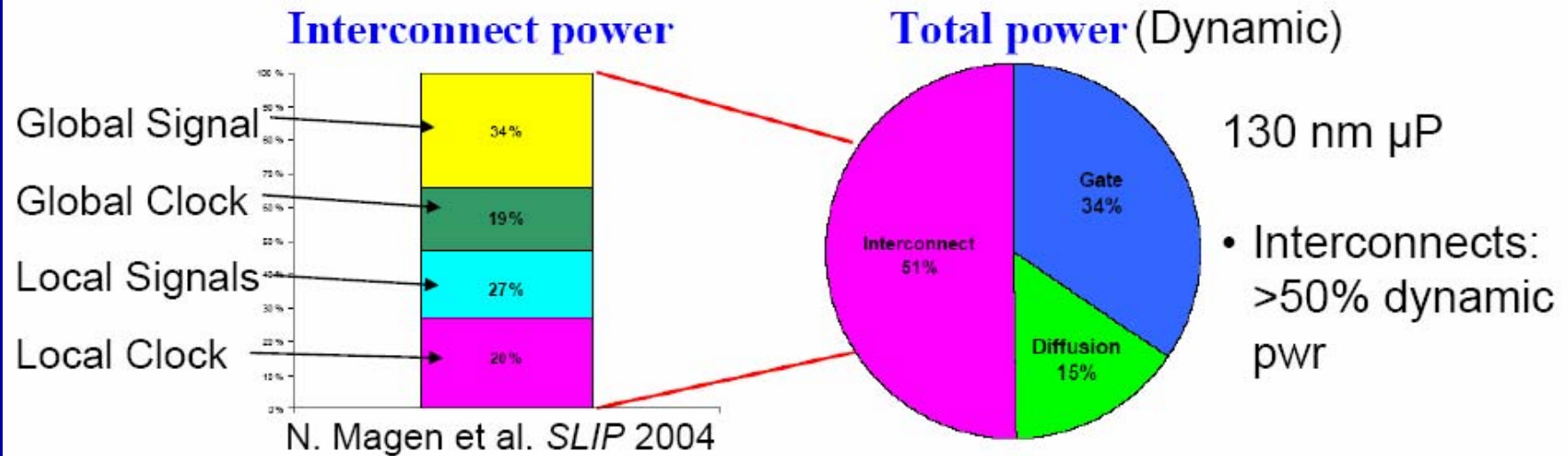
6/25/2009

Berkeley Symposium on Energy

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Performance tests/ratings are provided assuming specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. This data may vary from other material generated for specific marketing requests.

Sources of energy dissipation in PC

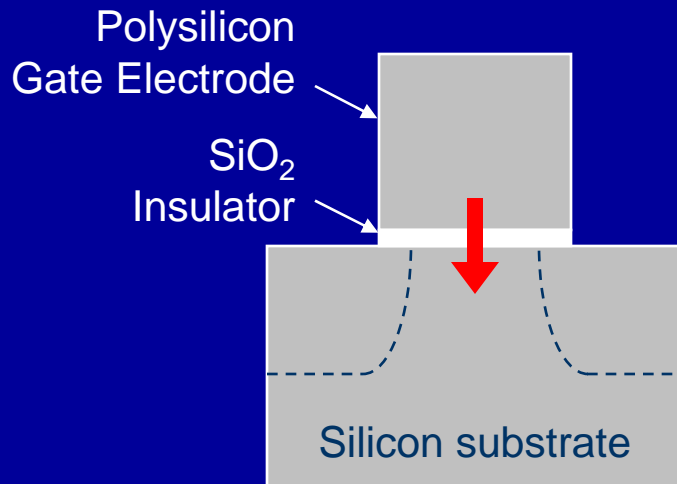


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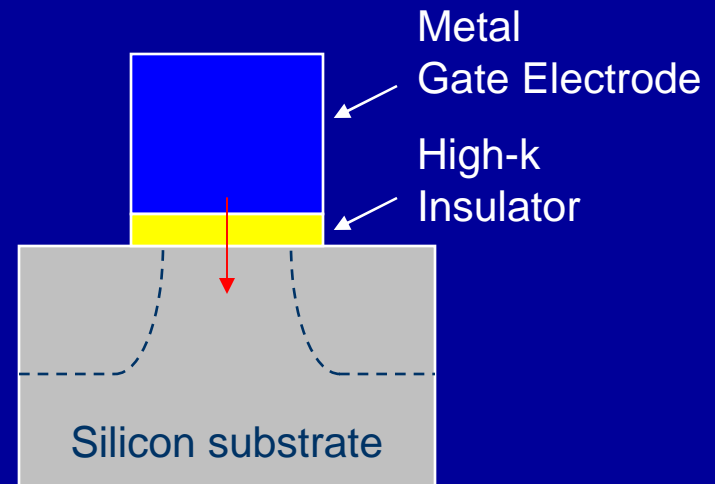
Transistor Scaling Challenges

Standard Transistor



Transistor scaling limited by SiO₂ gate insulator
Further SiO₂ scaling results in excessive gate leakage

High-k + Metal Gate

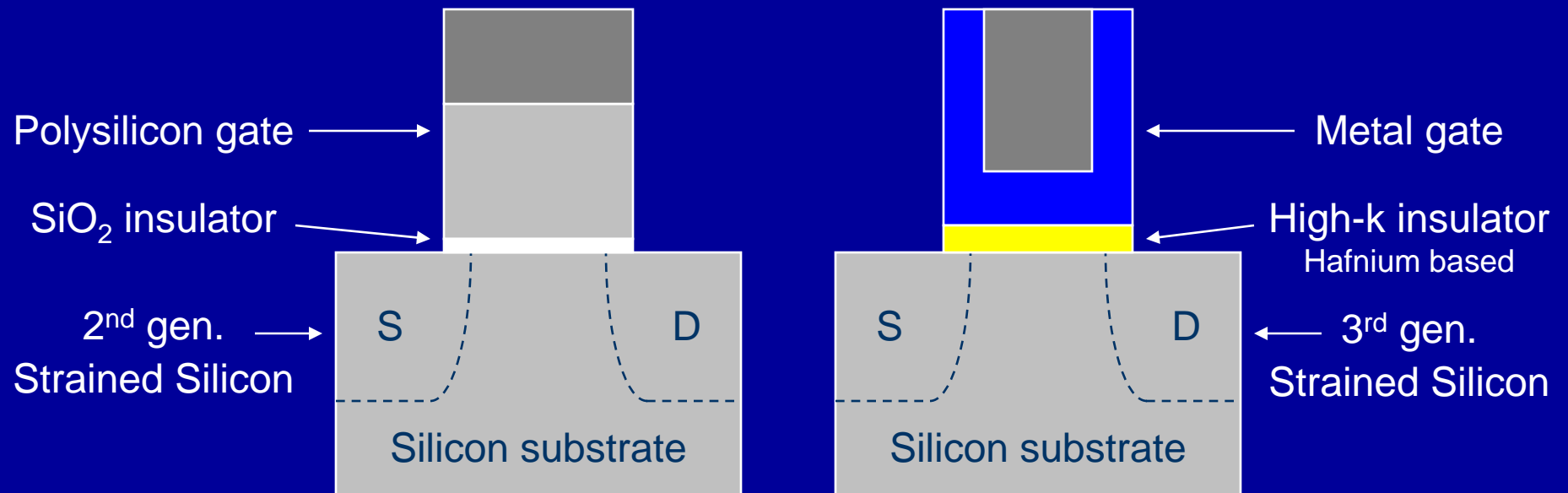


High-k + metal gate reduces gate insulator leakage and improves performance

Fundamental Change to Transistors

65 nm
Transistor

45 nm HK+MG
Transistor



Delivering Real Perf/Watt Improvement

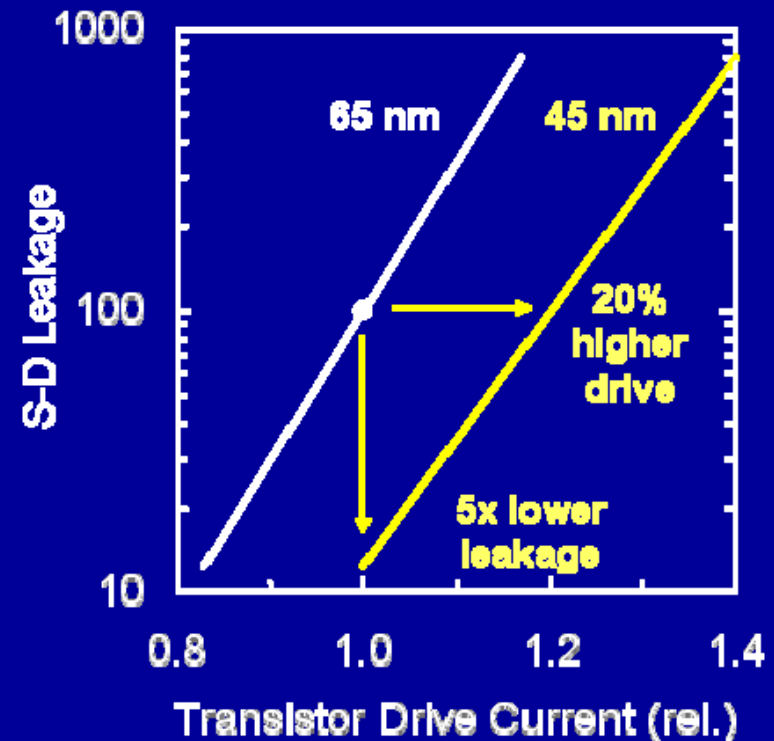
45 nm High-k + Metal Gate Performance / Watt Benefits

>10x lower gate insulator leakage

>30% lower switching power

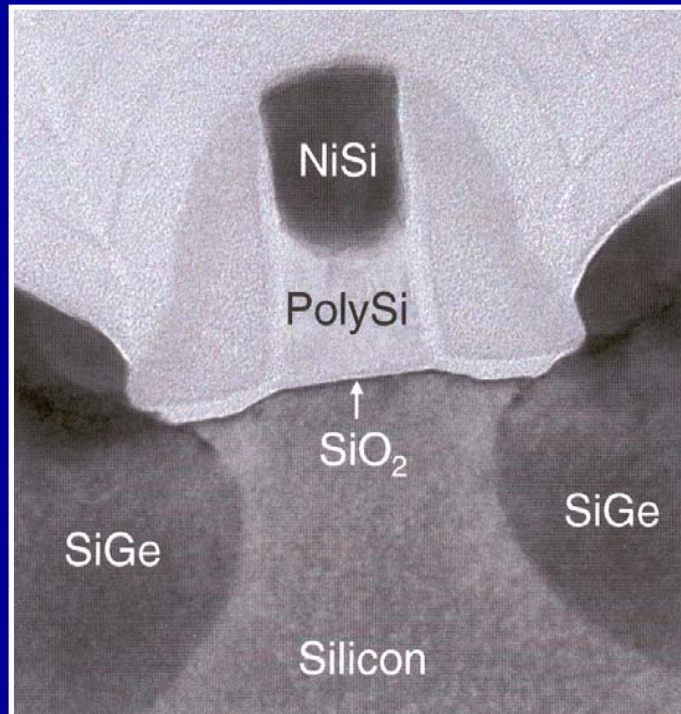
>20% higher drive current

>5x lower source-drain leakage

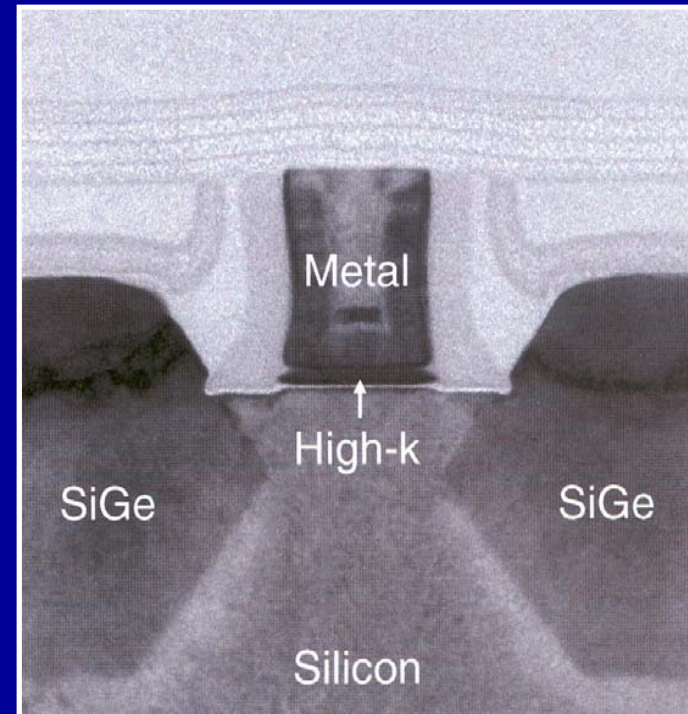


High-k + Metal Gate Transistors

65 nm Transistor



45 nm HK + MG



Hafnium-based high-k + metal gate transistors are the biggest advancement in transistor technology since the late 1960s

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Picking the Right High- μ Material

Material \Rightarrow Property \Downarrow	Si	Ge	GaAs	InAs	InSb
Electron mobility	1600	3900	9200	40000	77000
Hole mobility	430	1900	400	500	850
Bandgap (eV)	1.12	0.66	1.424	0.36	0.17
Dielectric constant	11.8	16	12.4	14.8	17.7

New Material Integration for High-Performance Transistors

N-channel built on Silicon (IEDM 2007)

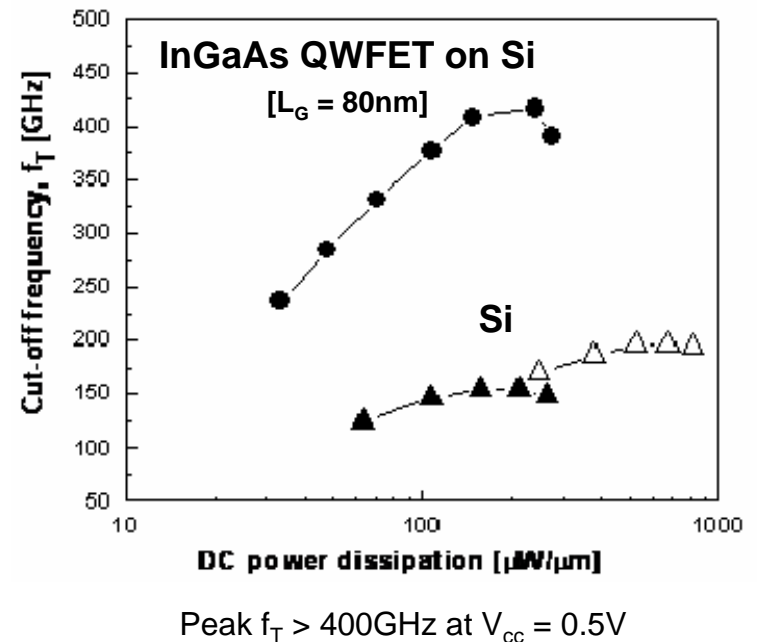
Background: III-V Integration with Silicon

Opportunity

- Higher mobility allows radical voltage scaling for 10x power reduction
- New material and deposition methods already in use starting with 45nm node

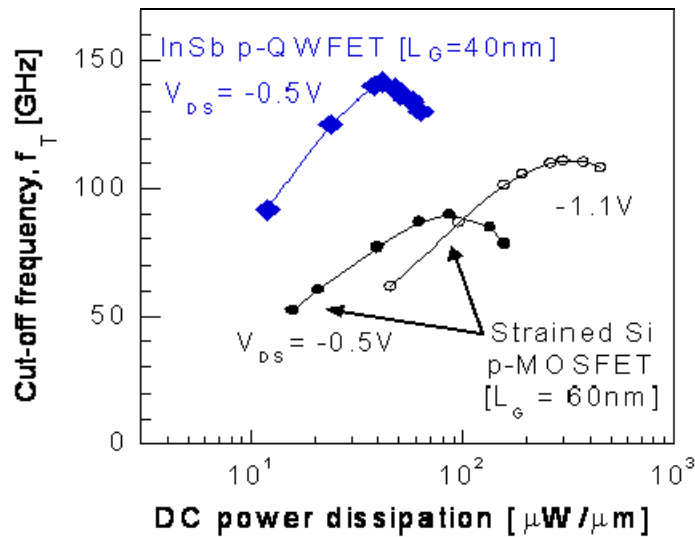
Key Challenges

- Integrate with Silicon Infrastructure
- Integration with Conventional Design
- Comparable Density and Cost

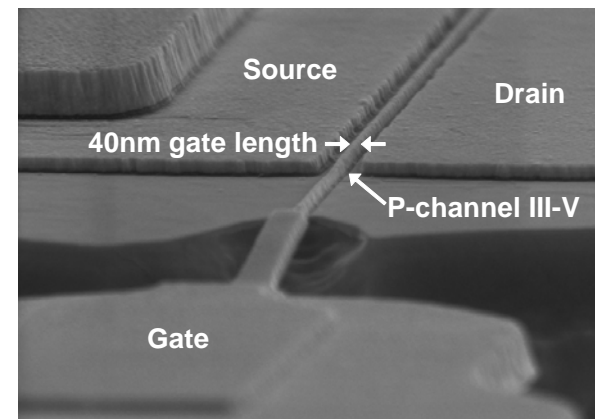
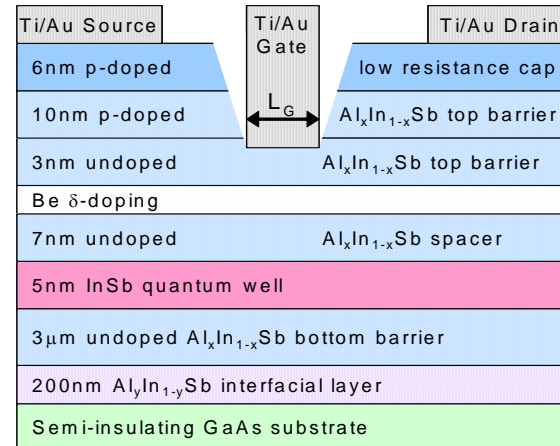


New Material Integration for High-Performance Transistors

P-channel with compressive strain (IEDM 2008)



Peak $f_T > 140$ GHz at $V_{cc} = -0.5\text{V}$



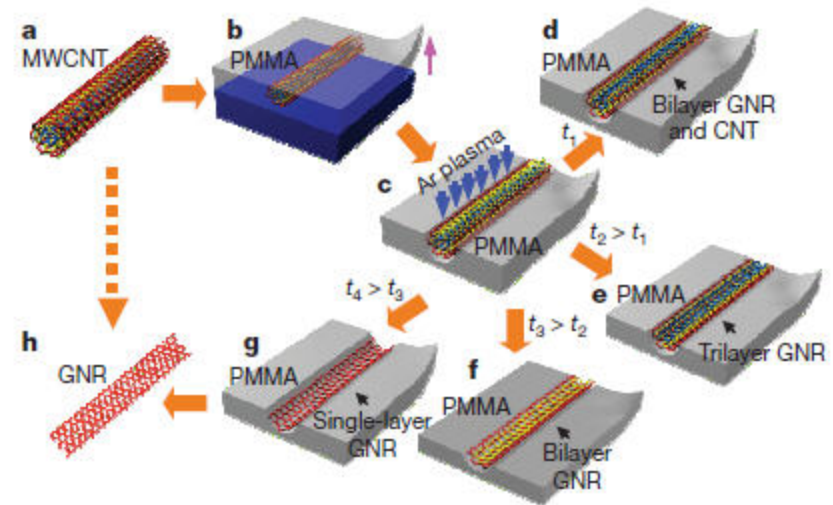
in partnership with Qinetiq

High performance III-V p-channel

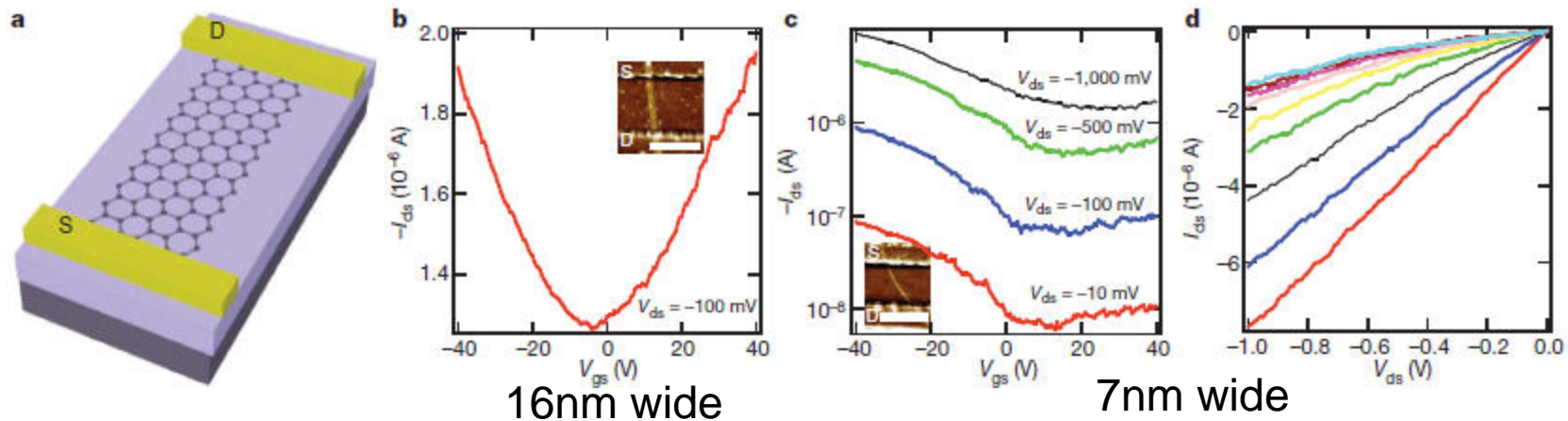
- Demonstrated with InSb
- Compressive strain to raise mobility
- 10x reduction in power vs equiv Si
- Highest performance P-channel reported to date

Graphene nanoribbons

- Lithographically defined graphene nanoribbons have poor control of width, high roughness => resistance.
- Method for unfolding of nanotubes to nanoribbons
- Well controlled nanoribbons for a transistor channel, gate effect demonstrated.



Unfolding carbon nanotube to nanoribbon

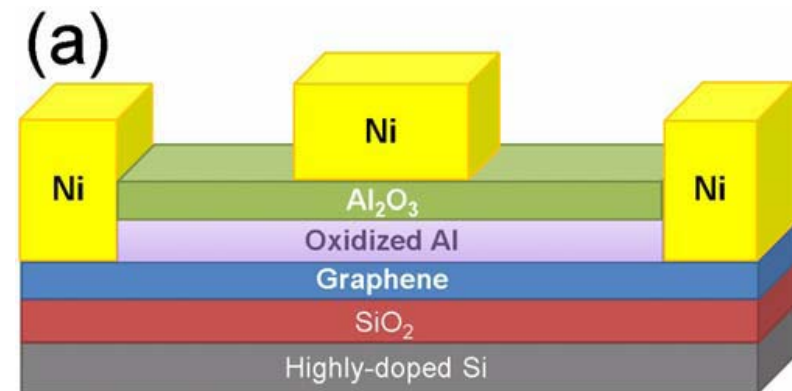


*Courtesy of Hongji Dai, Stanford. L.Jiao et al., Nature 458, 877 (2009).

High Mobility Top Gated Graphene FET

- High k dielectric of Al_2O_3 grown by ALD
- Thin Nucleation layer of Al deposited on graphene to facilitate adhesion of Al_2O_3 on graphene
- No degradation of electron mobility in graphene observed $\mu_e > 6,000 \text{ cm}^2/\text{Vs}$
- Impurity concentration on graphene surface $\sim 1.2 \times 10^{12}/\text{cm}^2$
- First demonstration of top gated graphene device devices without significant mobility degradation

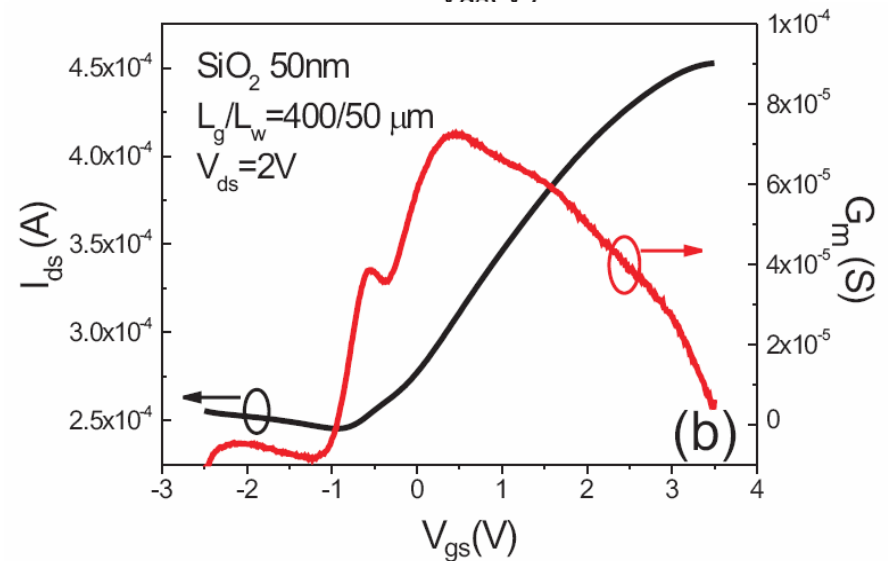
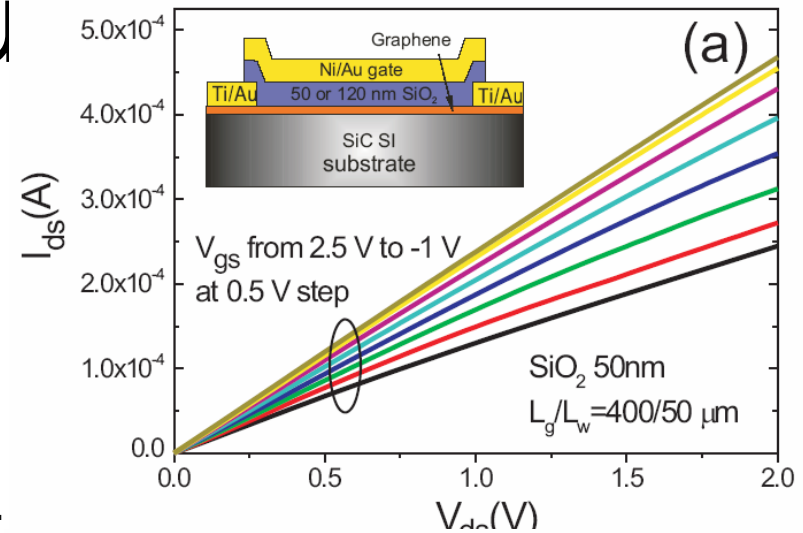
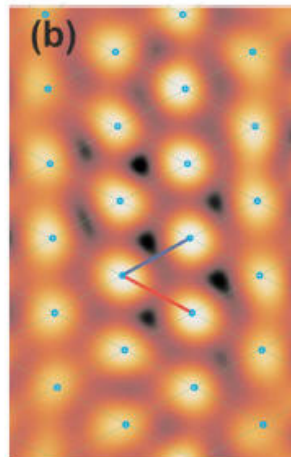
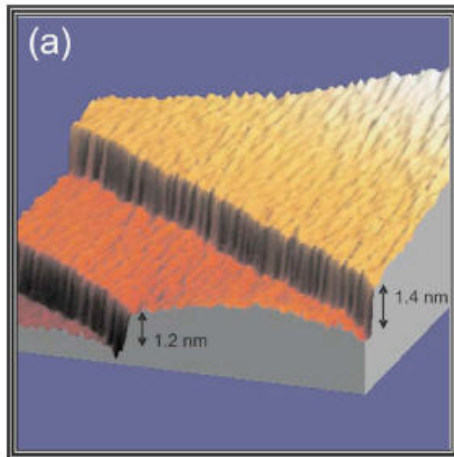
*Courtesy of Seyoung Kim et.al, U of Texas, Austin. S.Kim, Appl. Phys. Lett. 94, 062107 (2009).



Schematic of dual gated graphene FET

CVD graphene, transistor structure

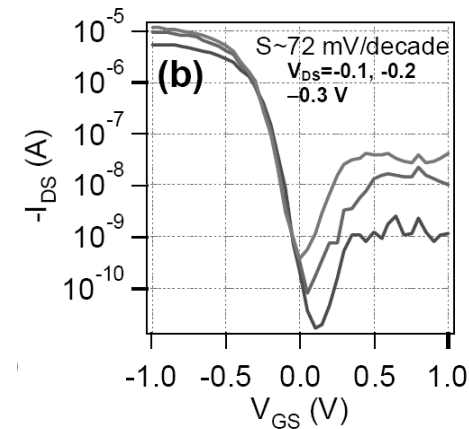
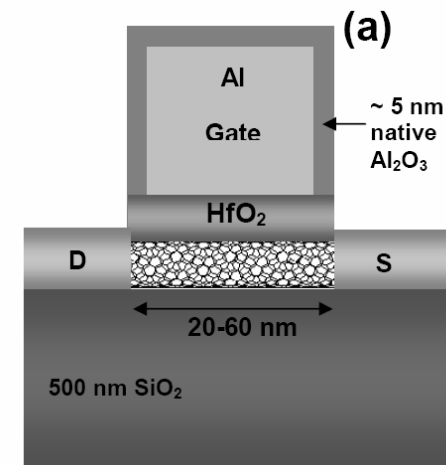
- Single crystal continuous graphene film grown by CVD on SiC, few monolayers. Proven by STM measurements.
- Developed gate dielectric on graphene preserving high mobility, ($5000\text{cm}^2/(\text{V}\cdot\text{s})$). Transistor structure – gate effect.
- Working on etch of nanoribbons width $<20\text{nm}$, for high-performance graphene FET.



*Courtesy of Jim Cooper, Purdue U. Y.Q.Wu et al., Appl. Phys. Lett. 92, 092102 (2008).

Room Temperature CNT FET

- 1.7 nm CNT
- Pd S/D contacts
- $T_{ox} = 8$ nm HfO₂
- Al top gate
- $I_{on}/I_{off} \sim 10^4$
- $SS \sim 72$ mV/decade
- MFP ~ 10 -15 nm at 2V

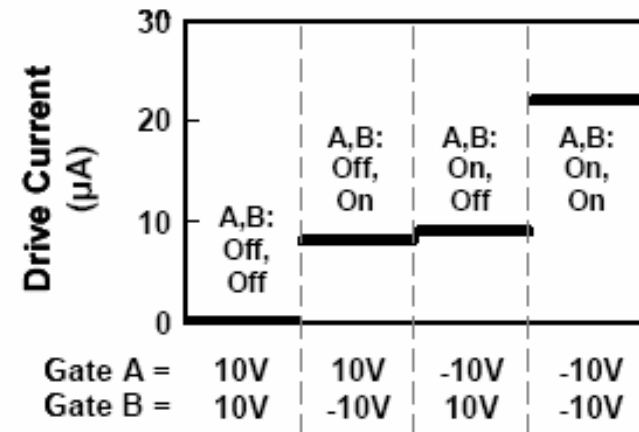
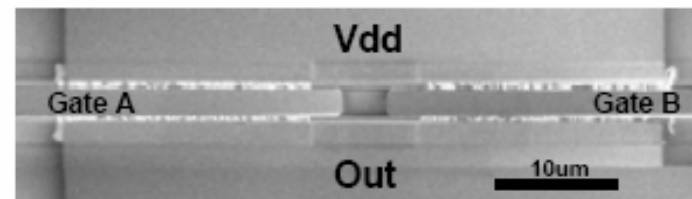
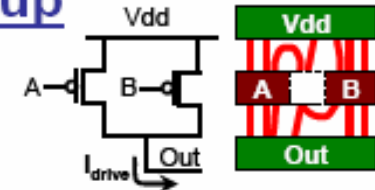


Misalignment immune CNT logic gates*

- First demonstration of full-wafer-scale growth of directional carbon nanotubes (CNTs) on 4" single-crystal quartz Wafers
- First demonstration of full-wafer-scale CNT transfer from 4" quartz wafers to 4" silicon wafers for integration on silicon
- Integration of full-wafer-scale growth and transfer, together with metallic-CNT removal
- First demonstration of misaligned-CNT-immune digital logic structures on a full-wafer-scale
- Increase CNT density needed

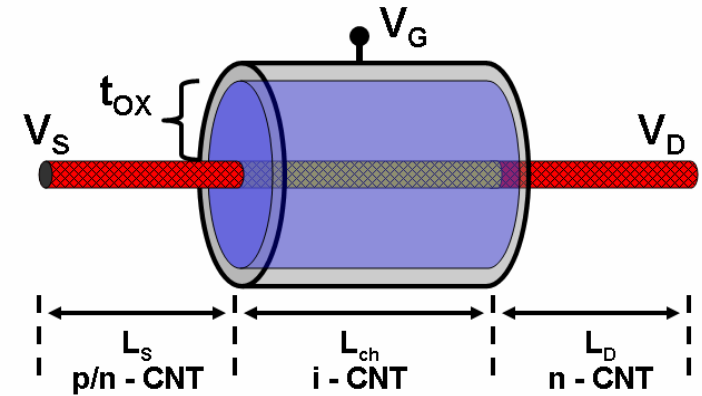
NAND Pull-up

$$\text{Out} = \overline{A \cdot B}$$

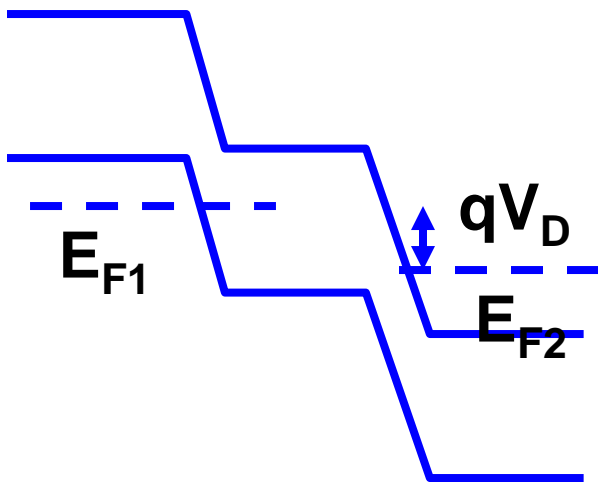


Tunneling transistor simulations

- Simulated and compared p-i-n and n-i-n carbon nanotube transistors **with scattering**. Subthreshold slope below 60meV/dec in tunneling transistor => lower voltage swing (0.3V).

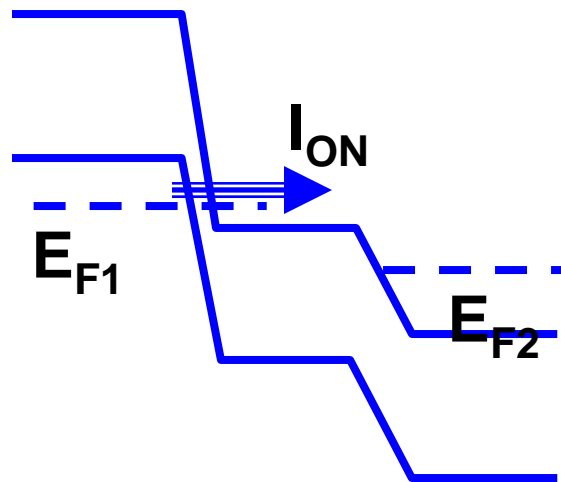


Band diagrams



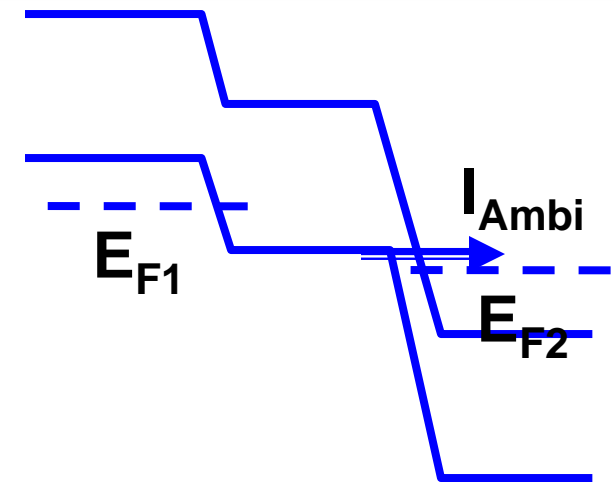
$V_G \sim 0, V_D > 0:$

OFF state



$V_G > 0, V_D > 0:$

ON state



$V_G \ll 0, V_D > 0:$

Ambipolar conduction

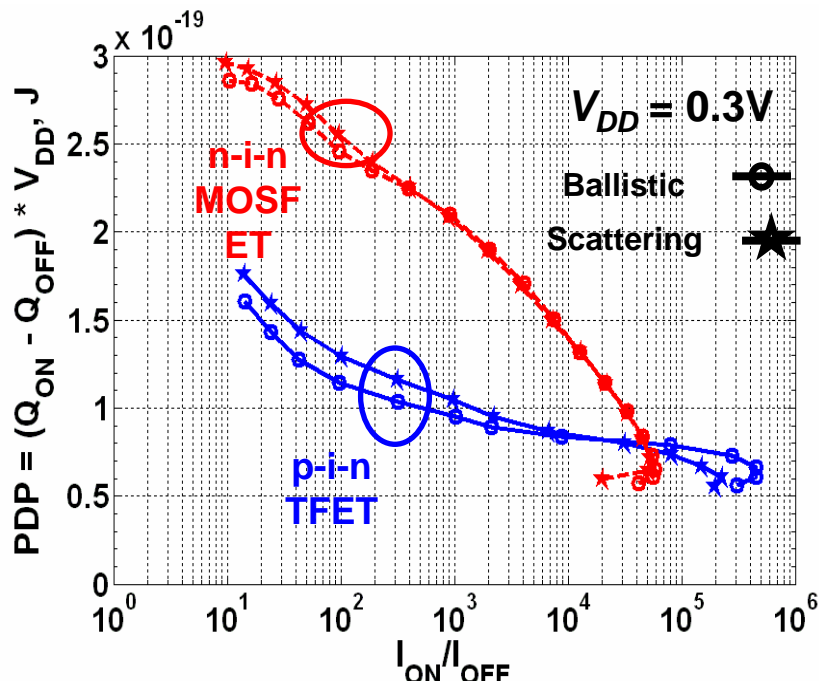
*Courtesy of Mark Lundstrom, Purdue U. S.Koswatta et al., IEEE TED 56, 456 (2009).

Tunneling transistor simulations

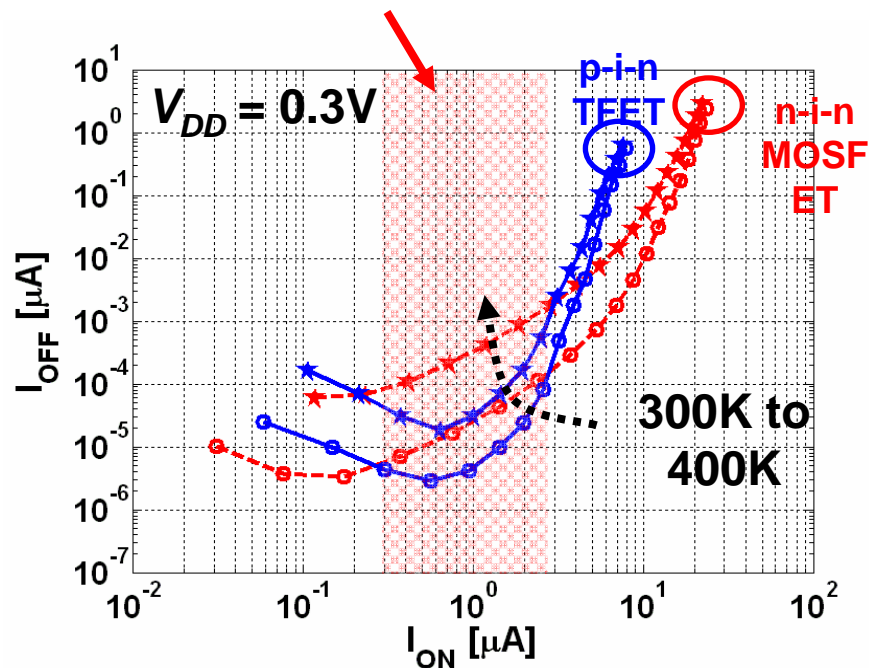
(2)

- Tunneling transistor is competitive with MOSFET for moderate on-current, show better switching energy due to inherently lower capacitance.

power-delay product=
switching energy



on-current where tunneling FET
has advantage



*Courtesy of Mark Lundstrom, Purdue U. S.Koswatta et al., IEEE TED 56, 456 (2009).

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Functionality based taxonomy of spin devices

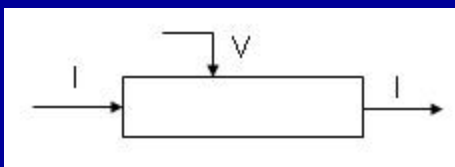


Fig 1A Data-Das modulator

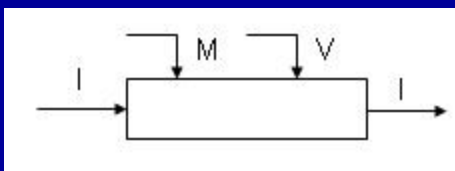


Fig 1B Spin FET

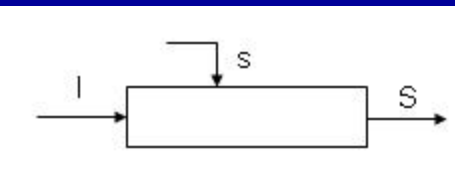


Fig 1C Spin Gain

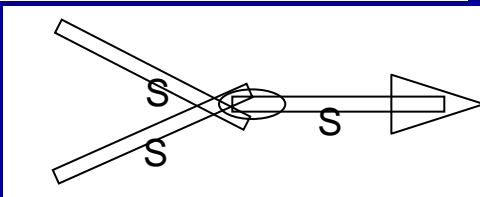


Fig 1D Spin Wave logic

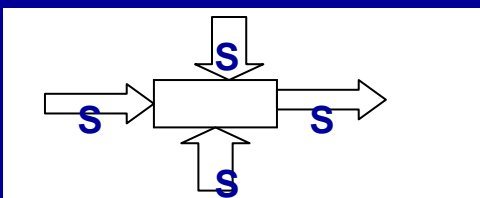
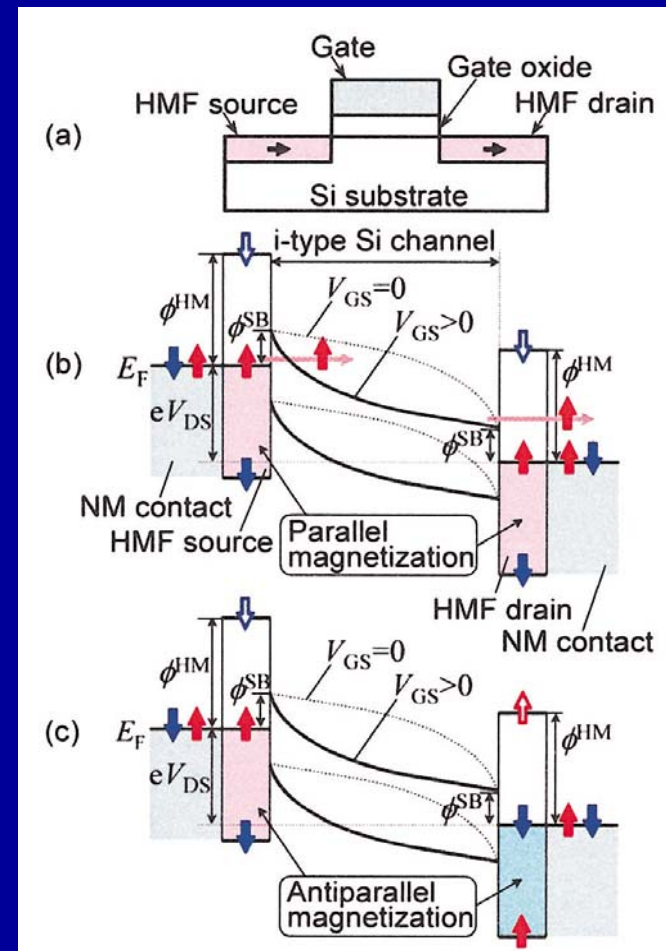


Fig 1E Domain Wall logic

Fig 1F Spin Torque logic

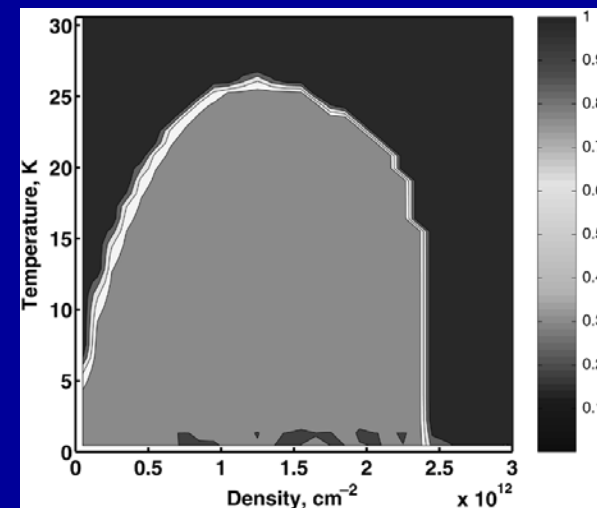
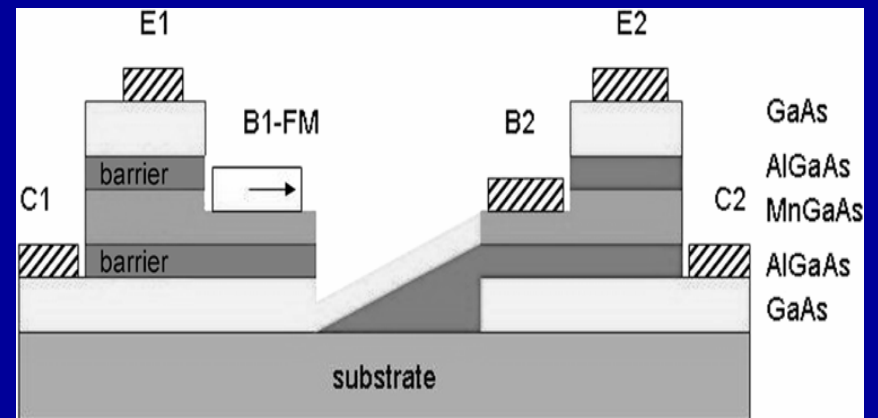
SPIN-FET*

- Large magnetocurrent ratio for nonvolatile memory and logic functions
- High transconductance for high speed operation,
- High amplification capability voltage, current and/or power gains to restore propagating signals between transistors,
- Requires room temperature half metal contacts
- small power-delay product and small off-current for low power dissipation



Spin gain device*

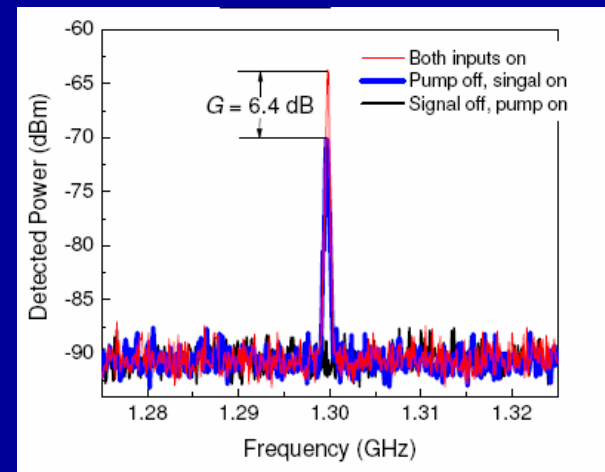
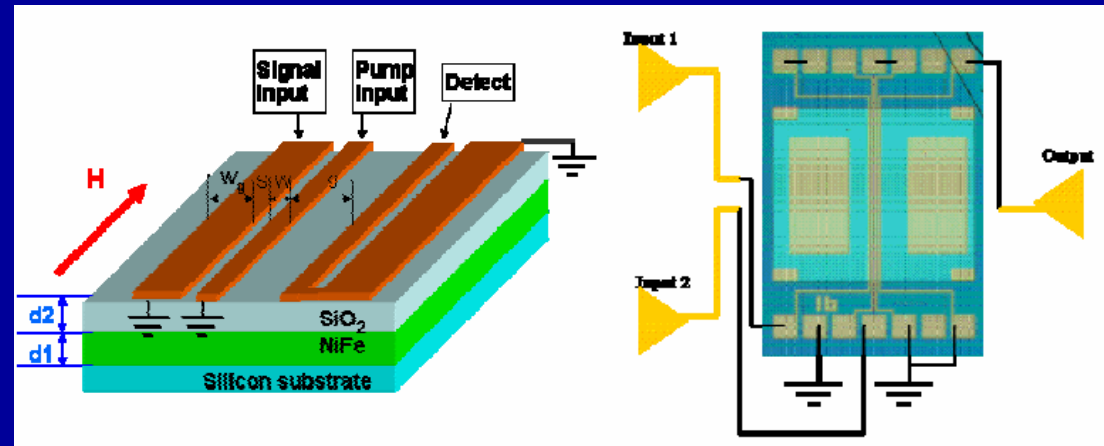
- Provides spin polarization gain
- Carrier induced spontaneous ferromagnetic transition
- MnGaAs with FM source drain



* Nikonov and Bourianoff, IEEE TRANSACTIONS ON NANOTECHNOLOGY, 6/25/2009, Berkeley Symposium on Energy Efficient Electronic Systems, VOL. 4, NO. 2, MARCH 2005

Spin wave amplifier -parametric*

- Input Power: 5.4 dBm @ 1.30 GHz
- Pump power: 16.0 dBm @ 2.60 GHz
- Bias magnetic field: 91.3 Oe.
- Output power increase: 6.4 dB @ 1.30GHz

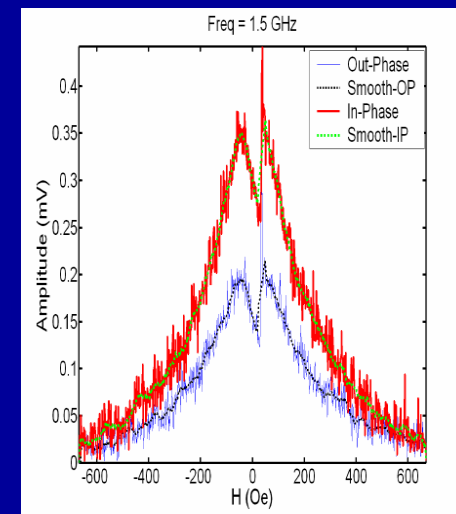
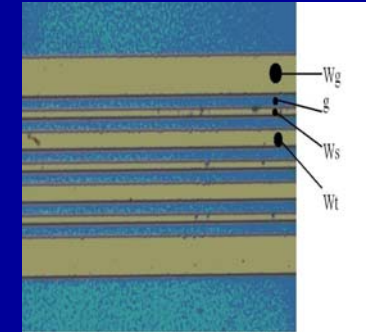
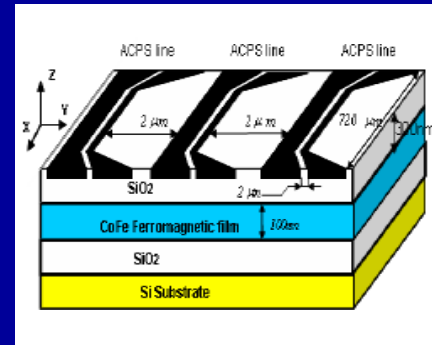


* A. Khitun, in press

6/25/2009

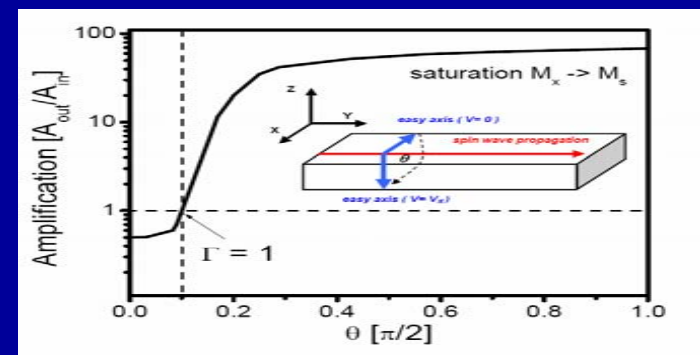
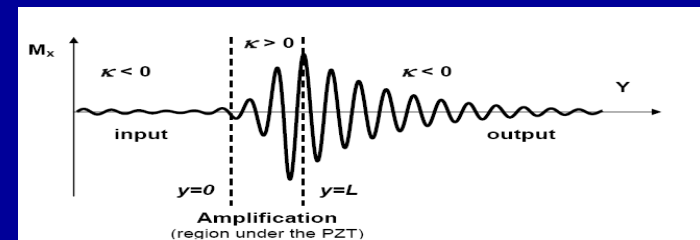
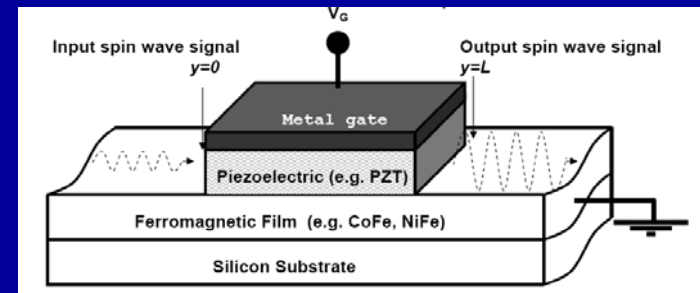
Spin wave interference device*

- Three terminal device
- In-phase/Off-phase ratio for 1.5GHz
- Bias magnetic field window (-650Oe > +650 Oe)
- All measurements at RT
- Gain ~ 3 DB



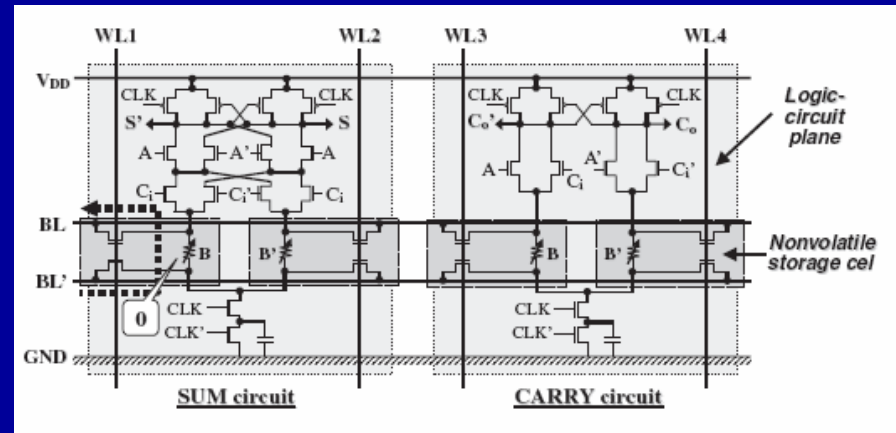
Spin wave amplifier – magnetoelastic *

- Two-phase multiferroic (PZT+CoFe)
- Coupling coefficient of 50mV/(cm×Oe)
- Coupling efficiency estimated to be 97%
- Bias field of 500 Oe
- Amplification ~30X



Full adder MTJ memory in logic

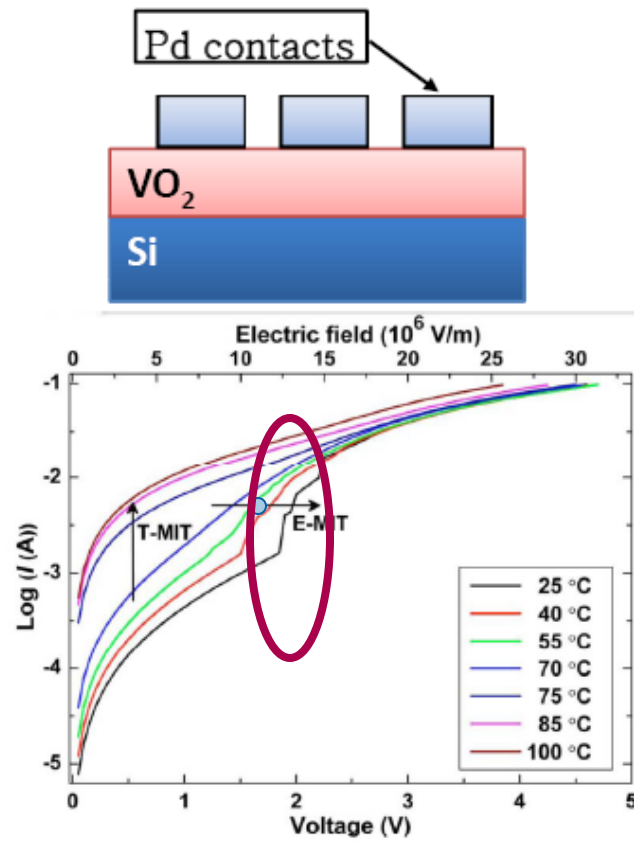
- Fabricated on 190 nm CMOS process
- MgO based MTJs
- Uses novel SyF layer to minimize J_c
- Dynamic power reduced >80%
- Static power reduced
- **Reduced component count**



	CMOS	Proposed
Delay	224 ps	219 ps
Dynamic power (@500MHz)	71.1 μ W	16.3 μ W
Write time	2 ns/bit	10 ns/bit (2 ns/bit) ^{a)}
Write energy	4 pJ/bit	20.9 pJ/bit (6.8 pJ/bit) ^{a)}
Static power ^{b)}	0.9 nW	0.0 nW
Area (Device counts) ^{c)}	333 μ m ² (42 MOSs)	315 μ m ² (34 MOSs + 4 MTJs)

Field induced phase transition in VO2 device*

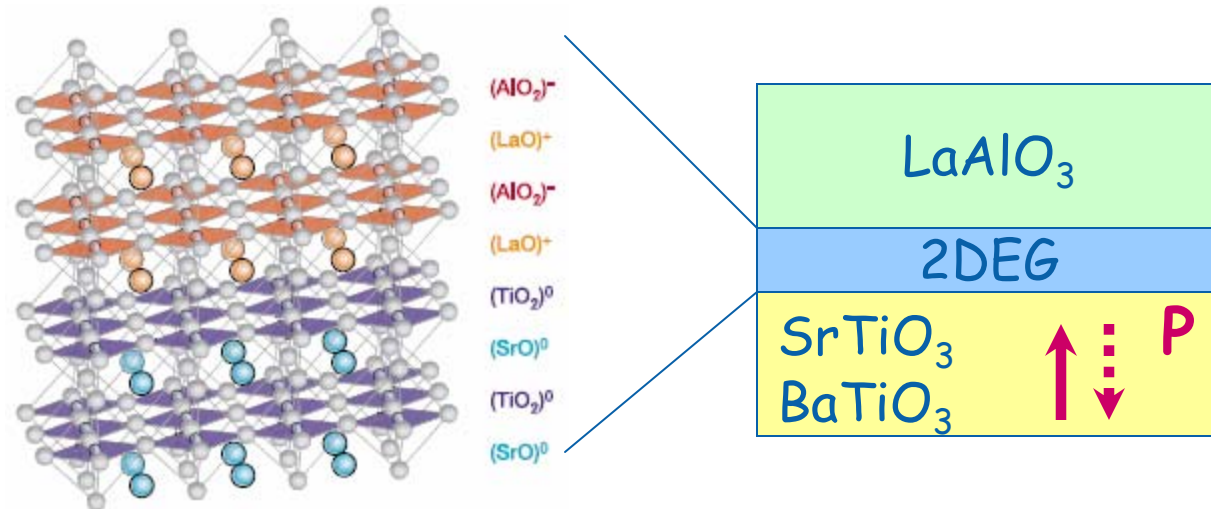
- Hall field measurements show 4 order of magnitude charge density increase at phase transition
- Room temperature, thin film measurement
- Differentiated from thermally induced transition by Raman measurements
- Potential for fast (>1 ps), 1V, RT MottFET device



Field-assisted phase transition seen across 150nm thick VO2 films grown on silicon at room temperature



Two-Dimensional Electron Gas Confinement at LaAlO₃=SrTiO₃ Interfaces*

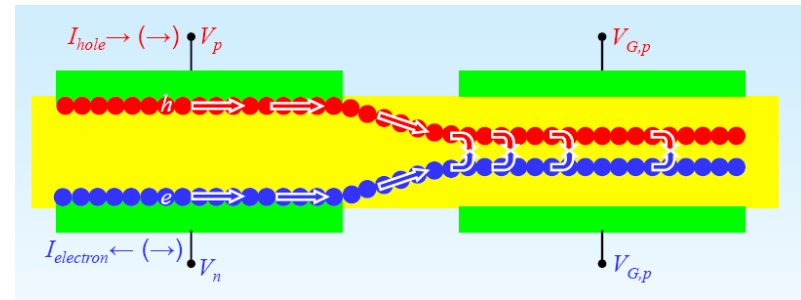


- 2 dimensional electron gas (2DEG) at the LaAlO₃/SrTiO₃ interface
- High charge density $>10^{14}$ /cm² – high mobility >100
- Polarization field determined by internal electric field
- Potential for a Ferroelectric Tunnel Junction
- Evidence for magnetism, both experimental and theoretical

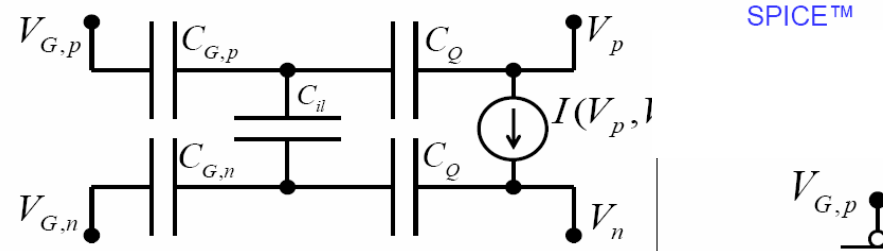
*Karolina Janicka, Julian P. Velev and Evgeny Y. Tsymbal, U of Nebraska

Bilayer pseudoSpin Field Effect Transistor (BISFET)

- Room temperature graphene is a gapless zero bandgap semiconductor with nearly identical conduction and valance bands
- Bilayer graphene structures can perhaps support excitonic electron-hole condensates
- Recombination of electron hole condensates can be controlled by applied gate voltages
- Spice model constructed that captures primary characteristics
- 100 GHz, 25mV operation with 5aJ per switching event



Gate controls interlayer tunneling between a p-type and an n-type graphene layer in the presence of an electron-hole exciton condensate.



Conclusions

- To extend Moore's law, Intel is addressing energy at all platform levels
- Intel is making steady progress in low power systems, platforms, and devices
- Intel is collaborating with the external research community to develop novel, beyond CMOS low power device research